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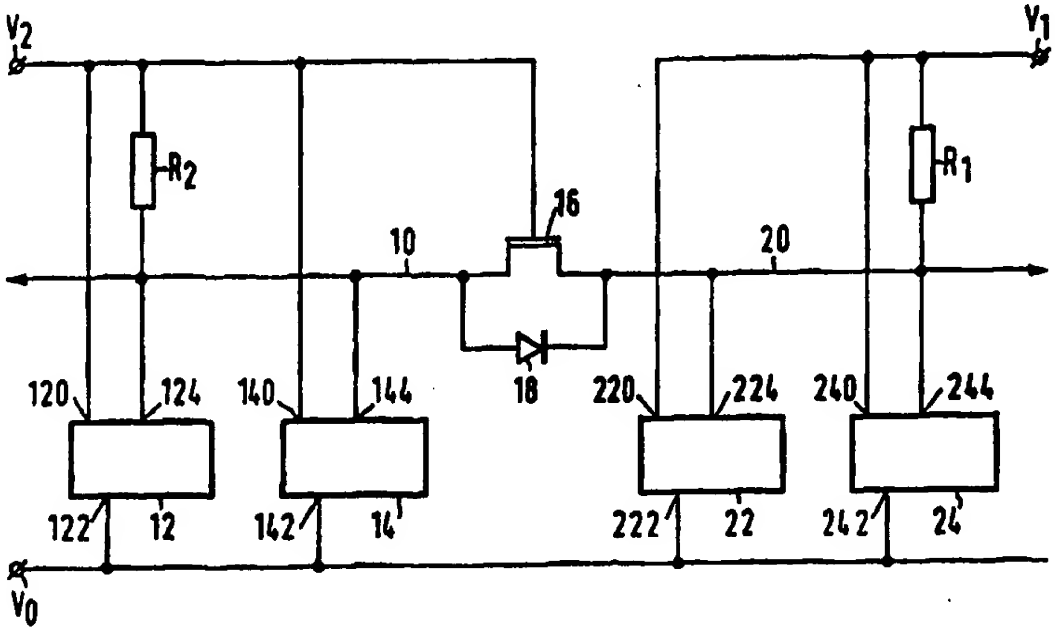

(57) Abstract

Information is supplied to a bus in a wired logic function, the potential on the bus either being pulled down to ground level or remaining at supply level. The data line in a bus is split into two parts which are interconnected via the main current channel transistor. Different supply voltages are used on the two parts. The control electrode of the transistor is connected to the lowest of the supply voltages. The transistor becomes conductive when either of the parts is pulled down. The transistor is non-conductive when none of the parts is pulled down.

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INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC6: G06F 13/40, G06F 1/32
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: G06F, H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 3832489 A (RALLAPALLI KRISHNA), 27 August 1974 (27.08.74), column 2, line 63 - column 3, line 29, see the figure	1
A	--	2-6
A	FR 2676559 A1 (MATRA DEFENSE), 20 November 1992 (20.11.92), page 3, line 26 - page 4, line 17, figures 1,2	1
A	--	2-6

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Patent Abstracts of Japan, Vol 13,No 543, P-970, abstract of JP, A, 1-224819 (HITACHI LTD), 7 Sept 1989 (07.09.89)	1
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A	IBM TECHNICAL DISCLOSURE BULLETIN, Volume 26, No 12, May 1984, (Armonk, New York, USA), T. Yanagi, "BUS EXTENSION SYSTEM" page 6481 - page 6483	1-6
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	EP 0549165 A2 (NATIONAL SEMICONDUCTOR CORPORATION), 30 June 1993 (30.06.93), column 2, line 25 - column 3, line 28	
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 3832489	27/08/74	NONE	
FR-A1- 2676559	20/11/92	NONE	
EP-A2- 0549165	30/06/93	JP-A- 5304722	16/11/93
		US-A- 5481222	02/01/96